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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,297	02/25/2002	Jean-Paul Theis		2037

7590 07/30/2004

AnteVista Gmbh
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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,297	THEIS, JEAN-PAUL	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The Oath or Declaration is objected to because of the following:

a. The Declaration filed February 25, 2002 fails to properly identify the International PCT Application Number as required by 37 CFR 1.63.

2. Appropriate correction is required.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claims 1 and 2 are objected to because of the following informalities:

i. Claim 1, line 5, the limitation "contains exclusively instructions" is obscure,

ii. Claim 1, lines 17 and 18, please change the limitation "(on said time axis)" to --on said time axis--,

iii. Claim 1, line 25, please insert a period after the limitation "format",

iv. Claim 2, line 2, please delete the extraneous period after the limitation "claim 1",

v. Claim 2, line 5, please change the limitation "(in cycle units of said clock)" to -- in cycle units of said clock --,

vi. Claim 12, line 9, please insert a period after the limitation "satisfied".

5. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Morrison et al., US Patent 4,847,755. Morrison et al. have taught a microprocessor having an instruction format containing explicit timing information (Figure 4, IFT),

a. where said instruction format refers to all the instructions being part of the instruction set of said microprocessor (Column 14, lines 6-14, Each instruction includes a firing time.),

b. where said microprocessor contains an instruction pipeline containing one or more stages (column 5, lines 9-24, column 36, lines 33-42),

c. where said machine code of said microprocessor contains exclusively instructions being part of said instruction set (column 2, lines 11-25),

d. where said microprocessor operates with a basic clock such that all time indications referring to instruction scheduling and execution as well as the depth of the instruction pipeline of said microprocessor are given in cycle units of said clock (column 5, lines 9-24),

e. where a time axis is defined by starting to count and label the clock cycles of said clock upwards from a certain point in time onwards or when microprocessor starts

operation and begins to execute the machine code of a given program (column 12, lines 40-60),

f. where instructions, being part of said machine code which is executed on said microprocessor, are pipelined such that instructions take one or more clock cycles to go through one or more stages of the instruction pipeline before completing execution (column 5, lines 9-24, column 36, lines 33-42),

g. where said timing information contained in the instruction format of an instruction contains one or more positive integer values representing delays according to which one or more entrance points (on said time axis) of said instruction into one or more pipeline stages have to be delayed either with respect to the point in time at which said instruction entered the previous pipeline stage or with respect to 'time zero' of said instruction, where the entrance point of said instruction into the first pipeline stage is delayed with respect to 'time zero', where 'time zero' is the point in time at which said instruction would enter the first pipeline stage in the absence of any delay (column 12, lines 40-60, column 14, lines 6-20, column, column 18, lines 10-31),

h. where said microprocessor contains some mechanism and hardware circuitry to delay the entrance points of the instructions into each pipeline stage according to the delays contained in the timing information of the instruction format (column 12, lines 40-60, column 18, lines 10-31).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable Morrison et al., US Patent 4,847,755, herein after Morrison et al., in view of Jovanovic, Zoran, et al., Software Pipelining of Loops by Pipelining Strongly Connected Components, 1991, IEEE, pages 351-365, herein after Jovanovic et al. Morrison et al. have taught a microprocessor having an instruction format containing explicit timing information as claimed in claim 1., as described above. Morrison et al. have not specifically taught where said microprocessor contains mechanisms and hardware circuitry to software-pipeline loops, that is

(a) to automatically start a new iteration of a given loop every p clock cycles, where p represents the initiation interval (in cycle units of said clock) and to overlap the scheduling and execution of said iterations of said loop

(b) for each iteration of said loop, to delay the entrance points of the instructions into the stages of the instruction pipeline according to the timing information contained in the instruction format of said instructions such that all resource constraints of said microprocessor are satisfied.

10. However, Jovanovic et al. have taught

(a) to automatically start a new iteration of a given loop every p clock cycles, where p represents the initiation interval (in cycle units of said clock) and to overlap the scheduling and execution of said iterations of said loop (abstract, page 352, section entitled "Loop optimizing algorithms at the fine grain level") for the desirable purpose of executing the optimal loop body pattern.

11. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the microprocessor of Morrison et al. contain mechanisms and hardware circuitry to software-pipeline loops, that is to automatically start a new iteration of a given loop every p clock cycles, where p represents the initiation interval (in cycle units of said clock) and to overlap the scheduling and execution of said iterations of said loop, as taught by Jovanovic et al., for the desirable purpose of executing the optimal loop body pattern.

12. Furthermore, this combination of Morrison et al. and Jovanovic et al. necessarily yields the following limitation

(a) for each iteration of said loop, to delay the entrance points of the instructions into the stages of the instruction pipeline according to the timing information contained in the instruction format of said instructions such that all resource constraints of said microprocessor are satisfied (The software-pipelined loop instructions of Jovanovic et al. will each include the timing information as each instruction in Morrison et al. includes a firing time. Morrison, Column 14, lines 6-14).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER